REMARKS

Claims 1, 2 and 4 through 23 are pending in this application. Claims 1, 7, and 15 are the independent claims. Claims 1, 7, 15 and 17 have been amended. Claim 16 has been cancelled without prejudice or disclaimer of the subject matter therein.

The Examiner has correctly noted that claim 18 was amended in Applicants' prior response to add the word "that" after "instruction" to overcome an objection and Applicants inadvertently did not underline "that" in the prior response.

The Examiner has objected to claims 10 and 19 under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Claims 20 and 21 have been objected to due to minor claim informalities. Claim 16 has been objected to due to allegedly not clearly limiting claim 15. Claim 16 has been cancelled without prejudice or disclaimer of the subject matter therein. Applicants respectfully traverse the objections to claims 10 and 19 through 21 and request reconsideration thereof for the following reasons.

The Examiner has rejected claims 1, 2 and 4 through 23 under 35 U.S.C. § 102(b) as being anticipated by Killian et al. (U.S. Patent No. 5,420,992). Applicants respectfully traverse the rejection and request reconsideration thereof for the following reasons.

Claim Objections

The Examiner has objected to claims 10 and 19 under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicants respectfully disagree. Claims 10 and 19 properly depend from and further limit the subject matter of their, respective, previous claims. Specifically, both claims 10 and 19 further limit claims 7 and 15, respectively, in that claims 7 and 15 both recite "an address format control

signal," and dependent claims 10 and 19 recite "an address format control flag," since a flag may store a signal and a signal may represent the value stored in a flag.

The Examiner also objected to claims 20 and 21 stating "the phrase 'an address format control flag' should be replaced with 'an address format control signal' based on the last paragraph on page 8 of the applicants [sic] remarks." Applicants respectfully disagree. The remarks the Examiner cites are made in reference to the address format control signal of claim 15, from which claims 20 and 21 depend, and not the address format control flag of claims 20 and 21.

The Examiner further objected to claim 16 not being clear as to whether it further limits claim 15. Applicants have withdrawn claim 16 without prejudice or disclaimer of the subject matter therein, and amended claim 17 to depend from claim 15.

Therefore, Applicants believe all of the objections to be overcome and respectfully request that all of the above objections be withdrawn.

35 U.S.C. § 102(b) Rejections

Claims 1 through 2, 4 through 15 and 17 through 23 are Patentable Over the Prior Art

Claims 1 through 2, 4 through 23 are rejected under 35 U.S.C. § 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992. Applicants respectfully traverse the rejection.

Referring to claim 1, the Examiner states that Killian has taught a processor comprising:

> "(a) means for executing an instruction of an application of a first bit size ported to a second bit size environment, the second bit size being greater than the first bit size. See column 2, lines 7-33.
> (b) means for confining the application to a first bit size address space subset (see column 19, lines 36-40), said means for confining comprising:
> (i) means for truncating generated address references of the second bit size to the first bit size. See column 10, line 62, to column 11, line 5. In this passage, Killian has explained that the 32-bit architecture ignores overflow (i.e., performs truncation)

during addition operations. Since Killian's system is backward compatible with the aforementioned 32-bit architecture, it follows that Killian's system would perform the same operations as the 32-bit architecture. Therefore, in overflow situations, truncation would be performed on 64-bit data (since the data path and register size of Killian's system is 64-bits) in order to obtain 32-bit data.

(ii) means for extending to the second bit size the truncated generated address references based at least in part on a setting of a predetermined control signal, the setting of the address format control signal to determine whether the truncated generated address references are to be zero-extended or sign-extended. See column 12, lines 45-65, and column 17, lines 27-31. The Examiner notes that 32-bit data is sign extended for use in the extended architecture. Also note that if the disclosed status register bits (address format control signal) specify 32-bit mode, the addresses are sign-extended from 32 bits to 64 bits. Otherwise, in 64-bit mode, no sign extension occurs. Therefore, it can be seen that the status register bits act as the applicants claimed address format control flag in that the setting of these bits determines whether the addresses are sign-extended or zero-extended. It should be realized that the applicant's use of the word "or" allows for anticipation by a reference which teaches either sign-extension or zero-extension (both do not have to be present to allow for anticipation).

Claim 1 has been amended to recite, *inter alia*:

"means for extending to the second bit size the truncated generated address references based at least in part on a setting of an address format control signal, a first setting of the address format control signal to indicate zero-extension of the truncated generated address references and a second setting of the address format control signal to indicate sign-extension of the truncated generated address references."

As a result, claim 1 now clearly recites that the "address format control signal" is to be used to both indicated when to zero-extend and when to sign-extend the address references. In contrast, in Killian et al., certain status register bits (i.e., the address format control flag) only control whether the address is sign-extended (see column 17, lines 27 through 31). Likewise, other status register bits (i.e., the address space control flag) determine which mode the processor is to operate in (e.g., user, supervisor or kernel modes) (see column 17, lines 25 through 27), and if user mode is specified, results in zero-extension of the address. (See column 3, line 67 through column 4, line 9.) However, neither set of status register bits in Killian et al., by themselves, can "indicate zero-extension of the truncated generated address references and . . . indicate sign-extension of the truncated generated

address references," as recited in claim 1 for the address format control signal. Therefore, there is no equivalent single structure in Killian et al. that is used to explicitly specify whether to zero-extend or sign-extend the truncated 32-bit addresses. Accordingly, the Section 102 rejection of claim 1 is believed to be overcome and Applicants respectfully request the Section 102 rejection of claim 1, and the claims that depend therefrom, be withdrawn.

Claims 7 and 15 have been amended to contain similar recitations as claim 1. Therefore, for at least those reasons given above for claim 1, Applicants also believe the Section 102 rejection of claims 7 and 15, and the claims that depend variously therefrom, have been overcome. Accordingly, Applicants respectfully request the Section 102 rejection of claims 7 and 15, and the claims that depend, respectively, therefrom be withdrawn.

Therefore, Applicants believe all currently pending claims to be allowable and respectfully request a notice of allowance to that effect be issued.

CONCLUSION

In view of the above amendments and remarks, the Applicants respectfully submit that the present case is in condition for allowance and again request that the Examiner issue a notice of allowance to that effect for all currently pending claims.

Applicants authorize the Commissioner to charge any fees determined to be due under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayment to Deposit Account No. 11-0600.

The Examiner is invited to contact the undersigned at (202) 220-4263 to discuss any matter concerning this application.

Respectfully submitted,

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